WHAT IS CLAIMED IS:

1. A semiconductor device including:

a semiconductor device die;

a heat-sinking support structure on which the semiconductor device die is disposed; and

nanotube regions containing nanotubes arranged on a surface of or in the heatsinking support structure or on the active device, the nanotube regions arranged to contribute to heat transfer from the semiconductor device die to the heat-sinking support structure.

2. The semiconductor device as set forth in claim **1**, wherein the semiconductor device die includes die electrodes arranged on the semiconductor device die, the heat sinking support structure further including:

contact pads defined by at least some of the nanotube regions, the contact pads electrically and mechanically contacting the die electrodes.

3. The semiconductor device as set forth in claim **2** wherein the contact pads further include:

a conductive coating disposed over the nanotube region

4. The semiconductor device as set forth in claim **3**, wherein the conductive coating includes:

an adhesion layer,

a barrier layer; and

a directly bondable layer disposed over the barrier layer.

5. The semiconductor device as set forth in claim **3**, wherein the conductive coating includes:

a gold layer thermosonically or thermocompression bonded with the die electrodes.

6. The semiconductor device as set forth in claim **2**, wherein the nanotubes of the contact pads are generally parallel to one another and extend away from the heat-sinking support structure.

7. The semiconductor device as set forth in claim **2**, wherein each contact pad includes:

a generally planar catalyst layer disposed on the heat-sinking support structure; and

generally aligned nanotubes that extend away from the catalyst layer.

8. The semiconductor device as set forth in claim **2**, wherein the semiconductor device die includes:

a light emitting diode device die having a flip-chip die electrode configuration.

9. The semiconductor device as set forth in claim **2**, wherein the nanotubes of the nanotube regions that define contact pads are predominantly nanorods.

10. The semiconductor device as set forth in claim **1**, wherein the heat-sinking support structure further includes:

microchannels arranged laterally in the support structure, at least some of the nanotube regions being disposed inside the microchannels.

11. The semiconductor device as set forth in claim **10**, further including:

a thermal transport fluid disposed in the microchannels.

12. The semiconductor device as set forth in claim **11**, further including:

an active cooling system that circulates the thermal transport fluid through the microchannels.

13. The semiconductor device as set forth in claim **12**, wherein the active cooling system is a recirculating active cooling system that includes a pump and a heat exchanger.

14. The semiconductor device as set forth in claim **10**, wherein the nanotubes disposed inside the microchannels are oriented generally perpendicular to the microchannels.

15. The semiconductor device as set forth in claim **14**, wherein the nanotubes are predominantly nanosprings.

16. The semiconductor device as set forth in claim **10**, further including:

a catalyst layer coating surfaces of the microchannels, the nanotubes disposed inside the microchannel extending generally away from the catalyst layer toward a center of the microchannel.

17. The semiconductor device as set forth in claim **10**, wherein the heat-sinking support structure further includes:

a first structure part with a first joining surface; and

a second structure part with a second joining surface parallel to the first joining surface, the first and second joining surfaces securely contacting one another, the microchannels being defined by grooves in at least one of the first and second joining surfaces.

18. The semiconductor device as set forth in claim **17**, wherein at least one of the first and second joining surfaces includes:

an oxide layer that anodically bonds the first and second joining surfaces together.

19. The semiconductor device as set forth in claim **10**, wherein the microchannels have a cross-sectional shape selected from a group consisting of circular, rectangular, square, triangular, octagonal, and pentagonal.

20. A method of fabricating a semiconductor device, the method including:

attaching a semiconductor device die to a die support; and

forming nanotube regions containing nanotubes on or in the die support, the nanotube regions being configured to conduct heat away from the attached semiconductor device die.

21. The method as set forth in claim **20**, wherein the forming of nanotube regions includes:

growing nanotube regions defining bonding bumps on the die support, the bonding bumps including nanotubes generally extending away from the die support, wherein the semiconductor device die is attached via the bonding bumps.

22. The method as set forth in claim **21**, wherein the forming of nanotube regions further includes:

depositing a catalyst layer on at least a portion of the die support, wherein the nanotubes of the bonding bumps selectively grow on the catalyst layer.

23. The method as set forth in claim **21**, wherein the growing of nanotube regions includes growing nanotubes that are predominantly filled nanorods.

24. The method as set forth in claim **21**, further including:

coating the bonding bumps with one or more metal layers to form metal-coated bonding bumps.

25. The method as set forth in claim **24**, wherein the attaching of the semiconductor device die to the die support includes:

thermosonically bonding die electrodes of the semiconductor device die to the metal-coated bonding bumps.

26. The method as set forth in claim **21**, wherein the semiconductor device die is a light emitting diode die, and the attaching of the semiconductor device die to the die support includes:

flip-chip bonding the light emitting diode die to the bonding bumps.

27. The method as set forth in claim **20**, wherein the forming of nanotube regions includes:

defining microchannels in the die support; and

growing nanotubes defining at least some of the nanotube regions inside the microchannels.

28. The method as set forth in claim **27**, wherein the microchannels are arranged to extend away from the attached semiconductor device die

29. The method as set forth in claim **28**, further including:

disposing a thermal transport fluid in the microchannels.

30. The method as set forth in claim **27**, further including:

flowing a working fluid through the microchannels.

31. The method as set forth in claim **27**, wherein the die support includes first and second wafers, and the defining of microchannels includes:

etching grooves in a joining surface of the first wafer; and

bonding the second wafer to the joining surface of the first wafer.

32. The method as set forth in claim **31**, wherein the bonding of the second wafer to the joining surface of the first wafer includes:

anodically bonding the second wafer to the joining surface of the first wafer.

33. The method as set forth in claim **20**, wherein the forming of nanotube regions includes:

depositing a catalyst layer on or in at least a portion of the die support; and

growing nanotubes on the catalyst layer.